JPL

Reliability Challenges for the Utilization of Non-Volatile Memories in Space Systems

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Sammy Kayali
Manager
Electronic Parts Engineering Office
Jet Propulsion Laboratory
California Institute of Technology
Tel. (818) 354-6830
Email:Sammy.A.Kayali@jpl.nasa.gov

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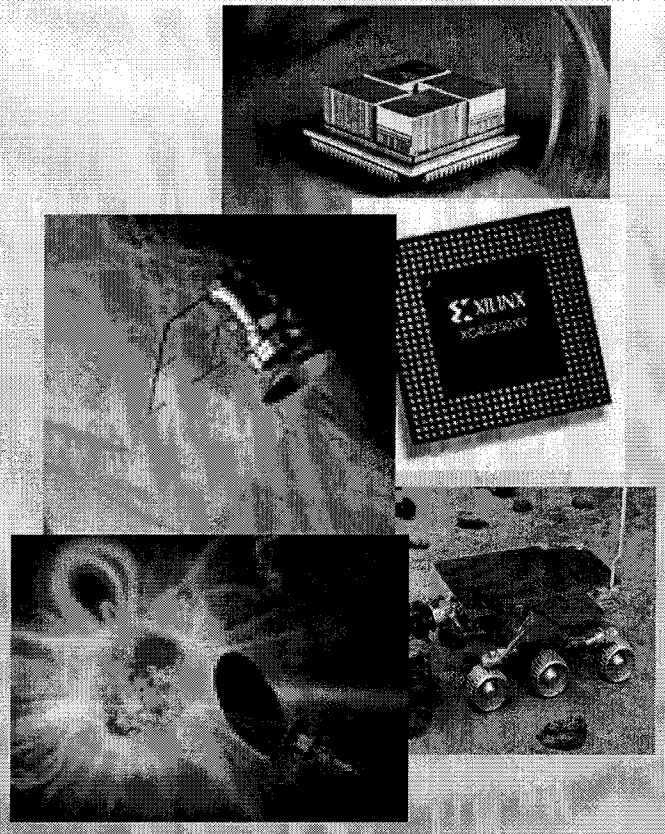
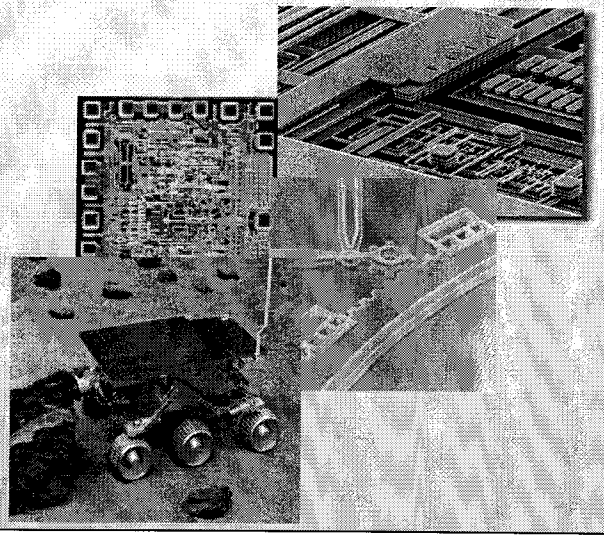
Overview

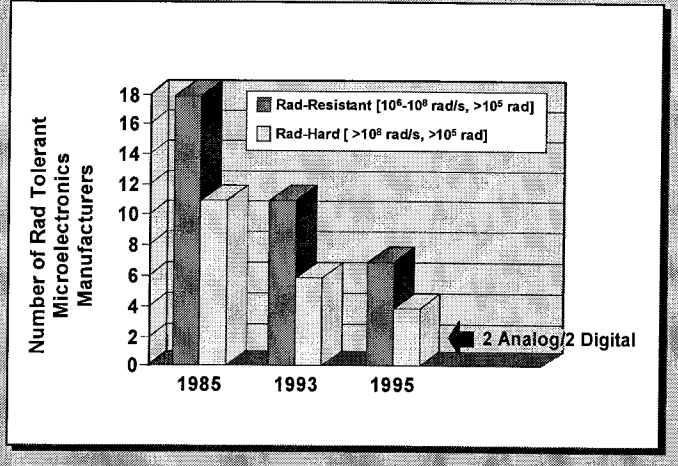
- *New system designs and performance requirements dictate the need to utilize high density memory devices.*
- *Power constraints necessitate the utilization of very low power electronics and retention of memory with no power*
- *The environmental requirements dictate the need to utilize radiation tolerant memory devices.*
- *Space systems must satisfy stringent reliability requirements*
- *Non-volatile memory technologies can provide promising solutions to address these issues*



Current Challenges

- *Technical challenges*
  - *Smaller feature sizes and miniaturization*
  - *Low power devices and processes*
  - *Device complexity*
  - *Radiation Tolerance of commercial Processes*
- *Environmental challenges*
  - *Operation at extreme temperatures*
  - *Reduction in mass and volume*
  - *New radiation effects and high radiation environments*
- *Programmatic challenges*
  - *Fast, better, cheaper missions*
  - *1/2 the cycle time, 2/3 the cost*
- *Industry challenges*
  - *Diminishing Hi-Rel suppliers*
  - *Lack of supporting military infrastructure and standards*
  - *Procurements for small volumes undesirable*





Current scientific trends

- *Experimenters needs set demands*
  - *Memory demands will increase*
    - *X2000 has 128 Mbytes per NVM slice*
  - *Missions will need faster processing*
    - *Memory will have to run faster and longer*
  - *Mission targets will become more remote or harder to attain*
    - *Pluto-Kuiper Express*
    - *Mars sample return*

Changing Applications for NVM

- *Long term retention*
  - *Missions will last >10 years*
  - *X2000 / PKE*
- *High endurance*
  - *Vehicle turned on rarely and exercised heavily*
  - *X2000 / Deep Impact*
- *Extreme thermal effects*
  - *Extreme temperatures*
  - *Prompt cycling between extremes*
- *Strict mission parameters*
  - *Low power*
  - *Low mass*
  - *High density*
  - *High data integrity*
- *Synergistic effects a factor*

NVM Types

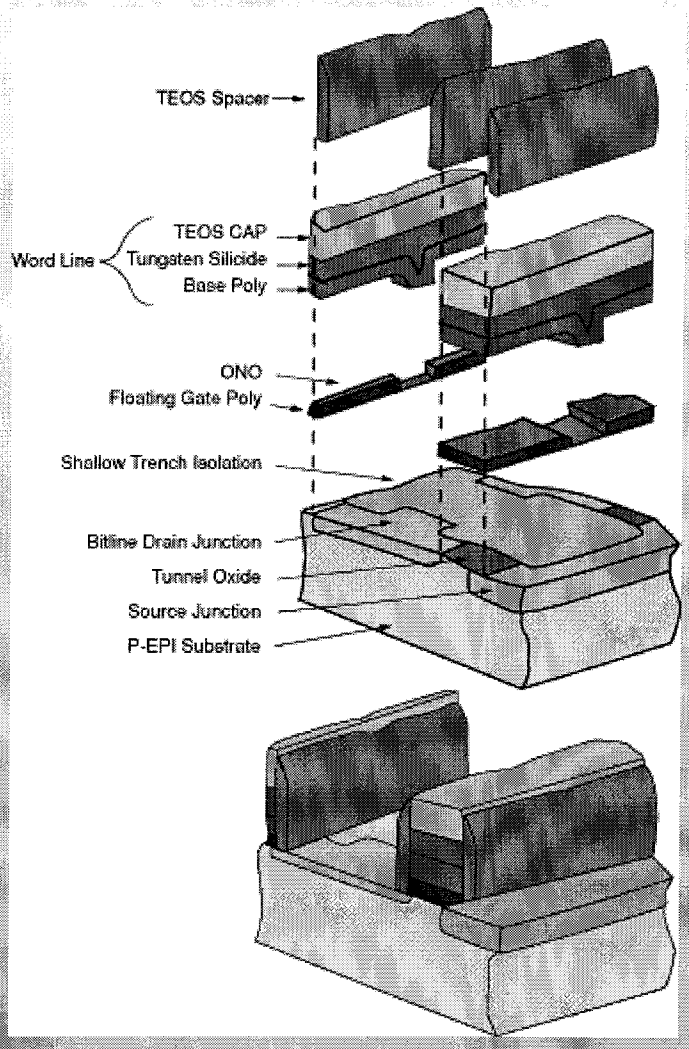
- *Charge Trapping*
  - *Floating Gate***
  - *Dielectric Trapping*
- *Field Polarization*
  - *Magnetic*
  - *Electric***
- *Phase Change*
  - *Chalcogenide*
  - *Anti-Fuse Technologies***
- *Circuit Based*
  - *Battery Backed-up SRAM* **

** *These devices are being flown on JPL missions.*

Charge Trapping

Floating Gate Structures

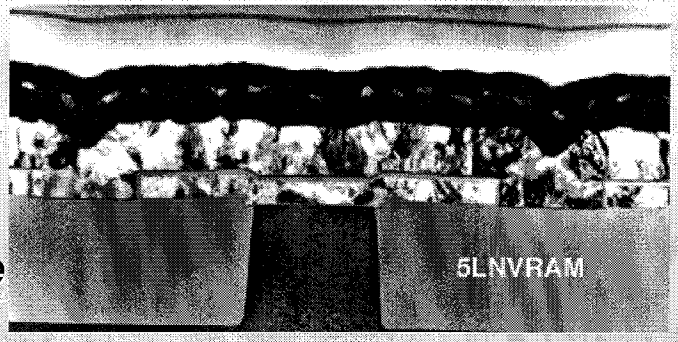
- *Based on the movement of electrons into and out of an isolated polysilicon structure "floating gate".*
- *Floating gate modulates the current flow through an associated FET*
- *Programming stores charge on floating gate*
- *Floating gate controls voltage threshold in transistor*
- *Can store more than one bit of information per transistor*
- *Electrical erase and write available*

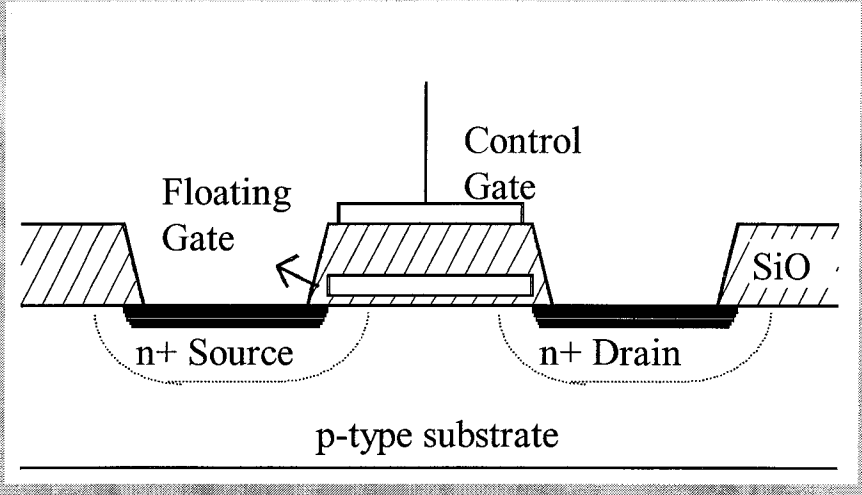


Charge Trapping

Floating Gate Reliability

- *Trap-up*
  - *Increase in voltage required to program/erase due to cycling*
  - *Can be enhanced due to radiation damage*
- *Charge pump degradation*
  - *Increase in leakage current and timing failure*
- *Time dependant dielectric breakdown*
- *Retention*
  - *10 yr. retention at 25C*
  - *135C retention down to 1 year*

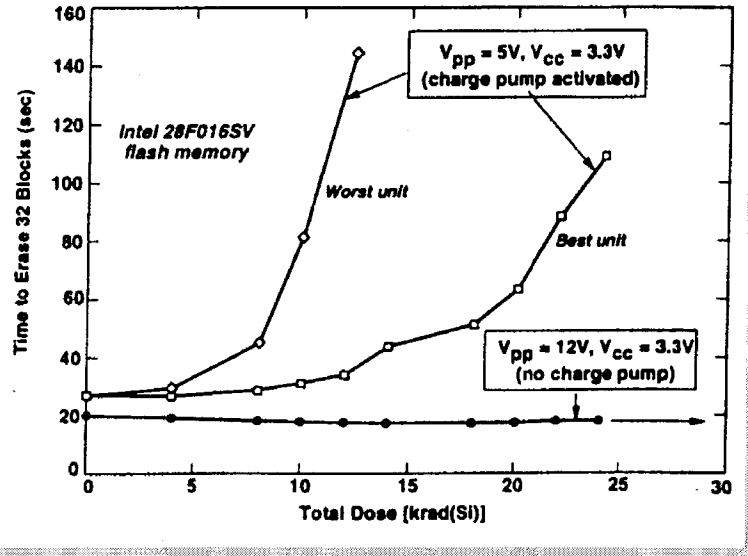




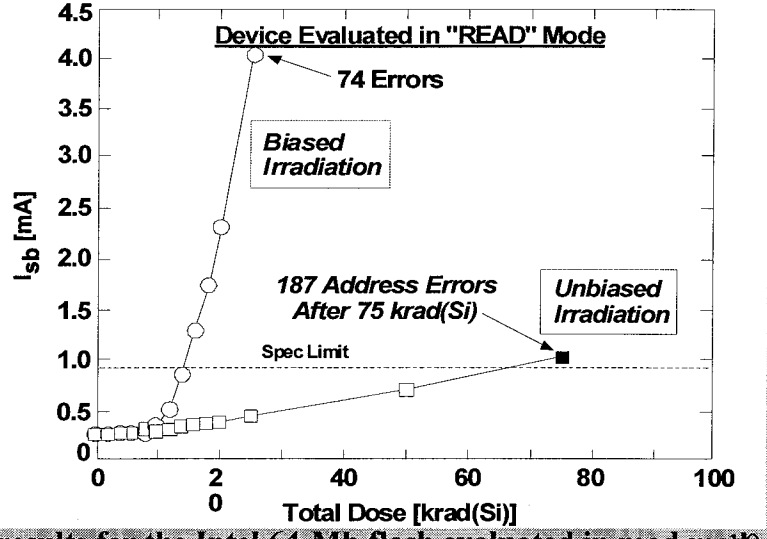
Charge Trapping

Floating Gate - Radiation Characteristics

- *Total Ionizing Dose Effects*
  - *Failures at 10krad levels due to charge pump mechanism*
  - *Failures at 50krad levels due to read sense amp*
  - *Failures at 100krad levels due to FG erasure*
  - *ELDRS may be a factor*



TID effect on time to program for various charge pump configurations.

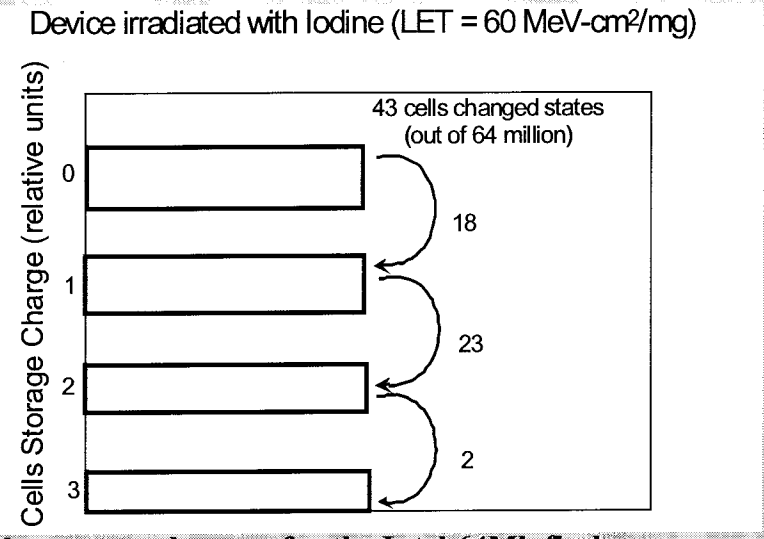


TID results for the Intel 64-Mb flash evaluated in read mode.

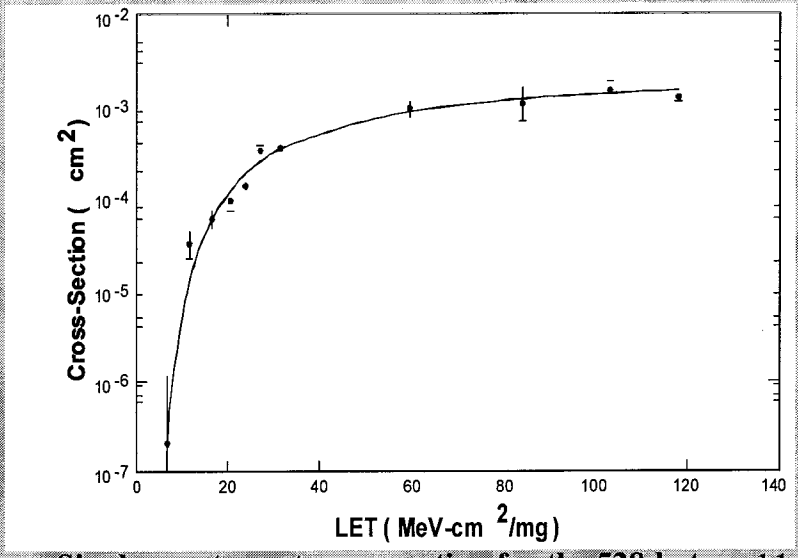
Charge Trapping

Floating Gate - Radiation Characteristics

- Single Event Latchup
  - Devices are very susceptible
- Single Event Upset
  - Single cell designs are mostly immune
  - Multi-level designs are susceptible
  - Buffers and registers are very susceptible



Single event read errors for the Intel 64Mb flash memory.

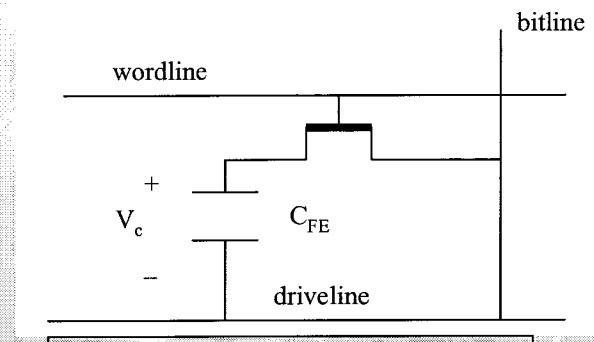


Single event upset cross-section for the 528-byte buffer register of the Samsung 128Mb flash.

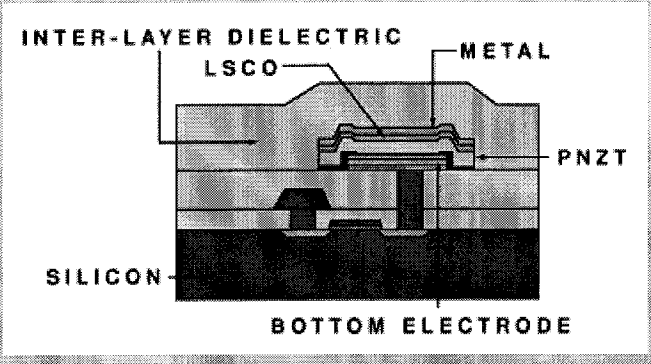
Field Polarization

FeRAM Structures

- *Utilize the bi-stable state of ferroelectric materials*
- *Apply external voltage to flip state*
- *Various materials have been utilized*
  - *SBT ($SrBi_2Ta_2O_9$)*
  - *PZT ($PbZr_xTi_{1-x}O_3$)*
- *Destructive readout (DRO) in 1T/1C design requires another cycle to rewrite*



Simplified 1T/1C FeRAM Cell

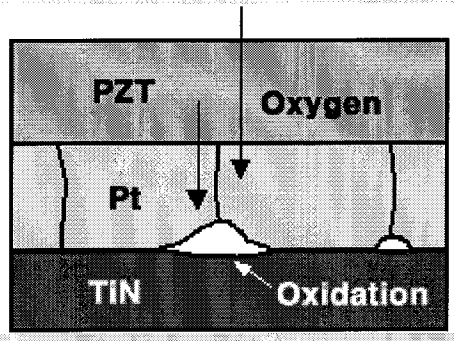


Cross Section of FeRAM Cell
Source: Radiant Technologies, Inc.

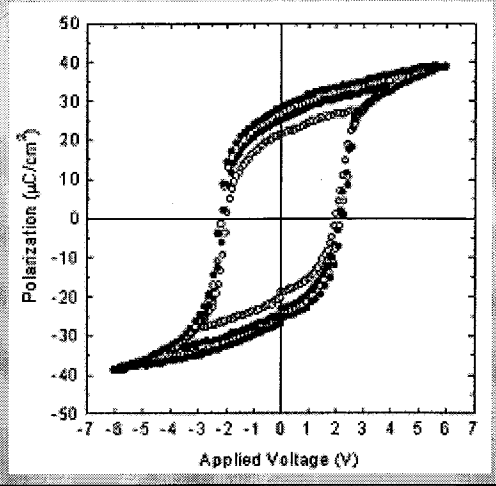
Field Polarization

FeRAM Reliability

- *Fatigue*
  - *Gradual Loss of remnant polarization due to wear*
- *Aging*
  - *Degradation of parameters with time*
- *Time Dependant Dielectric Breakdown (TDDB)*
- *Imprint*
  - *Ferroelectric develops preference for state if left in state for long period*
- *Relaxation Phenomenon*
  - *Increase in time required for state settling after continuous cycling*
- *High temperature will wipe memory*
- *Hysteresis threshold shift in 1T/1C*
  - *The polarization will shift with use causing threshold to be outside sense amp range*



Oxidation of TiN barrier layer
INOSTEK Inc.

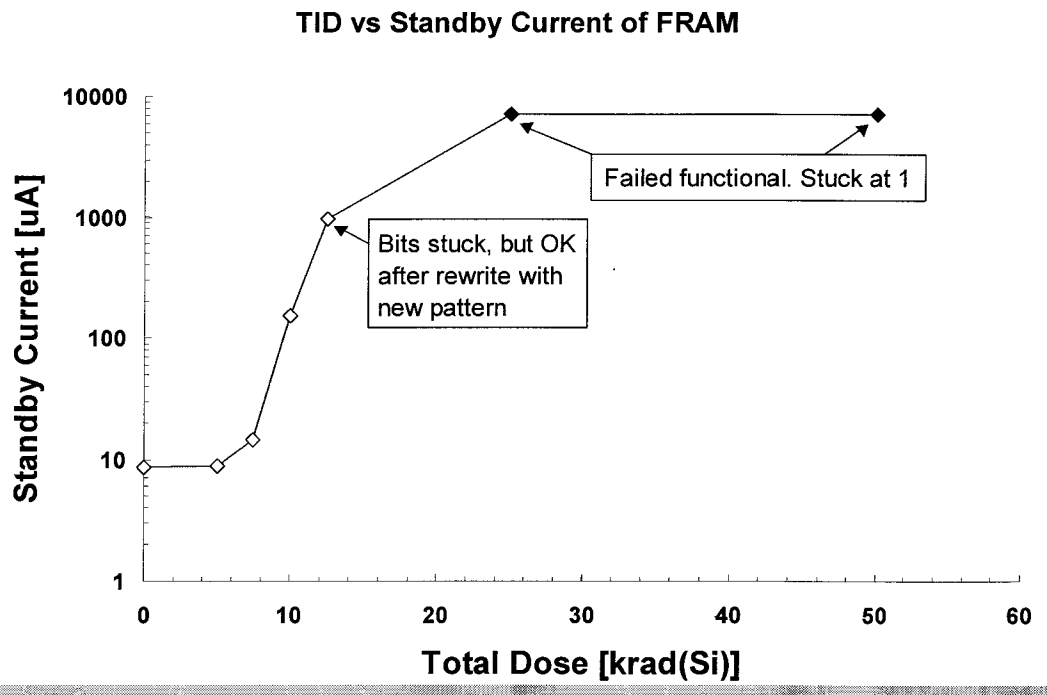


P-V hysteresis of Pt/PZT/INOSTEK/Pt/TiN
INOSTEK Inc.

Field Polarization

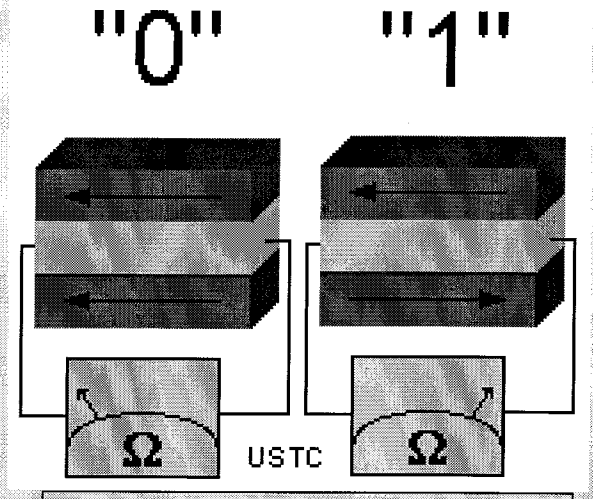
FeRAM Radiation Characteristics

- *Total Ionizing Dose*
  - *CMOS supporting circuitry show failures at about 25krad*
  - *ELDRS may be a factor for peripheral circuitry*
  - *Some reliability issues are accelerated with radiation*
- *Single Event Latchup*
  - *Devices are very susceptible*
- *Single Event Upset*
  - *Cells appear immune*
  - *DRO may increase miswrite cross section*

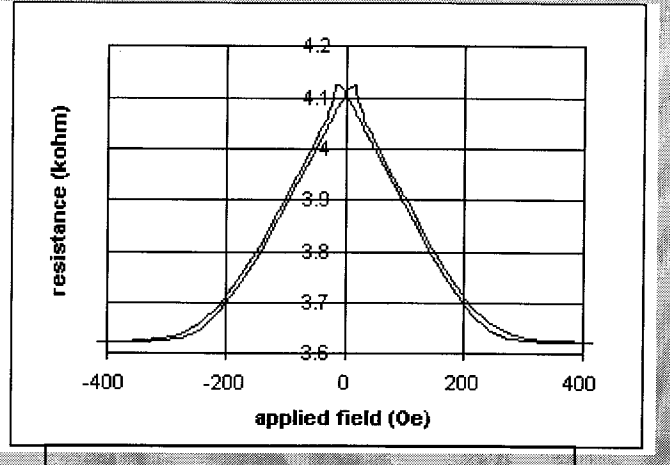


Field Polarization

- ***Magneto-resistive Memory (MRAM)***
- *Uses Anti-parallel Magnetic Fields to Limit Current in Cell*
  - *Electron spin scattering*
  - *1T/1C possible*
  - *DRO and non-DRO*
- *High permutation of cell structures and approaches*
  - *MRAM*
  - *SDT*
  - *Spin Valve*
  - *Pseudo-Spin Valve*



Simplified Magneto-Resistance Cell
USTC Inc.



GMR Response of Multilayer Cell
NVE Inc.

Field Polarization

MRAM Reliability

- *No devices available to test*
  - *Reliable survey limited*
- *High temperature should affect memory*
- *Hysteresis threshold shift in 1T/1C*

MRAM Radiation Effects

- *CMOS presents usual problems*
  - *SEL*
  - *Leakage*
- *Interface issues*
  - *Displacement damage*
- *Field Issues*
  - *EMP*

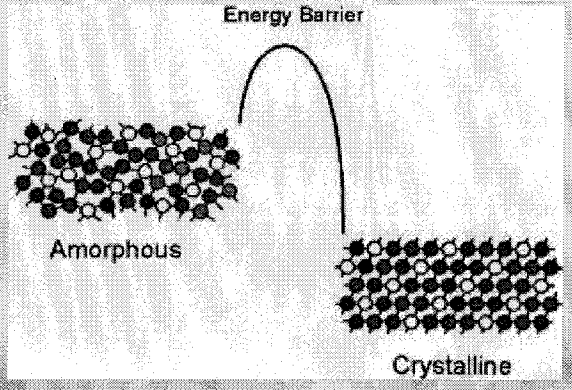
Phase Change Memories

Anti-Fuse

- *Alters resistance of current path*
- *One time program*
- *Alpha-Silicon, Alpha-Carbon or ONO*

Chalcogenide

- *Alters Resistance of current path in material*
- *Provides for ~10^2 change in resistance*
- *Provides High rewrite*
- *New Technology*



Phase change process
ECD, Inc.

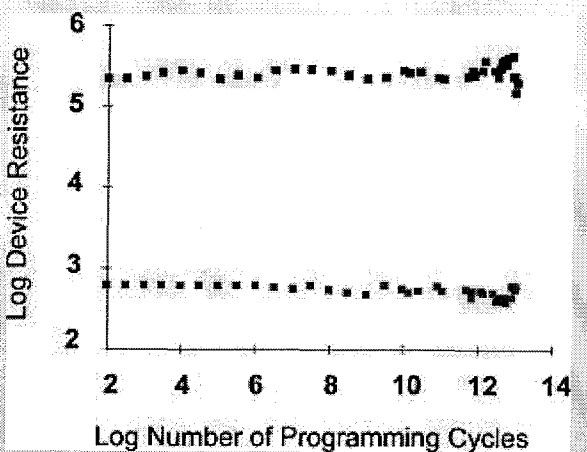
Phase Change Memories

Chalcogenide Reliability

- *Limited reliability data is available on Chalcogenide memory devices*

Antifuse Reliability

- *On State Breakdown Reliability*
  - *Current stress on programmed state leads to open circuit*
  - *MTTF ~ 1/V*
- *Off State Switching*
  - *Inadvertent switching from programmed state to non programmed state due to high field*



Rewrite cycles for Chalcogenide memory
ECD, Inc.

Phase Change Memories

Chalcogenide Radiation Characteristics

- *No commercial product has been available for test*
- *CMOS structures are expected to suffer typical leakage current degradation*
- *Devices expected to be susceptible to Single Event latchup and Upset due to CMOS support circuitry*
- *Current dependence of read and write mode may lead to enhanced radiation sensitivity*

Anti-Fuse Radiation Characteristics

- *Commercial CMOS Structure is expected to suffer typical leakage current degradation*
- *Rad hard and Rad tolerant device are available*
- *Un-programmed and partially programmed anti-fuse resistance is expected to increase under biased irradiation*
- *Devices expected to be susceptible to Single Event latchup and Upset*

Summary

- *New space systems require the utilization of high density memory devices with proven reliability*
- *Current commercial technologies do not satisfy the density, radiation tolerance, or endurance requirements for space applications*
- *FeRAM technology appears the most promising in the near term*
- *Chalcogenide memory device technologies offer great potential for low power operation and radiation tolerance, but requires further development.*
- *MRAM still under development*

Current Status of NVM

	FeRAM	MRAM	FLASH	EPRPOM	C-RAM	SRAM	DRAM	IDEAL
Non-Volatile	Yes	Yes	Yes	Yes	Yes	No	No	Yes
Power Consumption	Low	Low	Med	Med	Med(?)	Med	High	Low
Stand-by Power Consumption	Low	Low	High	High	Low	Med	High	Low
Operating								
Write Speed	<150ns	<1μs(?)	>10μs	<10μs	<60ns(?)	<10ns	<60ns	<60ns
Erase Speed	<150ns	<1μs(?)	>10ms	>10s	<60ns(?)	<10ns	<60ns	<60ns
Write Voltage	~2-5V	~2-5V	>12V	>12V	~2-5V	~2-5V	~2-5V	~2-5V
Endurance	10^{12}	10^{10}	10^{6}	10^{5}	10^{13}	10^{15}	10^{15}	10^{15}
Read threshold	~50 mV	~5 mV	5 V	5 V	N/A	5V	5 V	~1 V
Cost/Bit	High	High	Med	Med	High	Med	Low	Low
Scale(Bits/Dev)	10^{4}	10^{4}	10^{8}	10^{5}	10^{7}	10^{7}	10^{8}	10^{9}
SEU susceptible (bit)	No	No	Yes	No	No?	Yes	Yes	No
SEU susceptible (periph)	Probably	Probably	Yes	No	Yes?	Yes	Yes	No
SEL susceptible	Yes	Probably	Yes	Yes	Yes?	Yes	Yes	No
TID krad(Si)	20	N/A	10	100	N/A	100	100	1000
Retention 25C (Yr.)	>10	>10	10	10	>10	0	0	>10
Retention 170C (Yr.)	0	N/A	1	1	>10	0	0	>10
Space worthy	Marginal	Maybe	Marginal	No	Maybe	N/A	N/A	Yes